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MANUFACTURING METHODS AND TECHNOLOGY (MM AND T) MEASURE FOR FAB--ETC(U)
AUG 77 R M HOPKINS, S W KESSLER, R E REED DAAB07-76-C-8120

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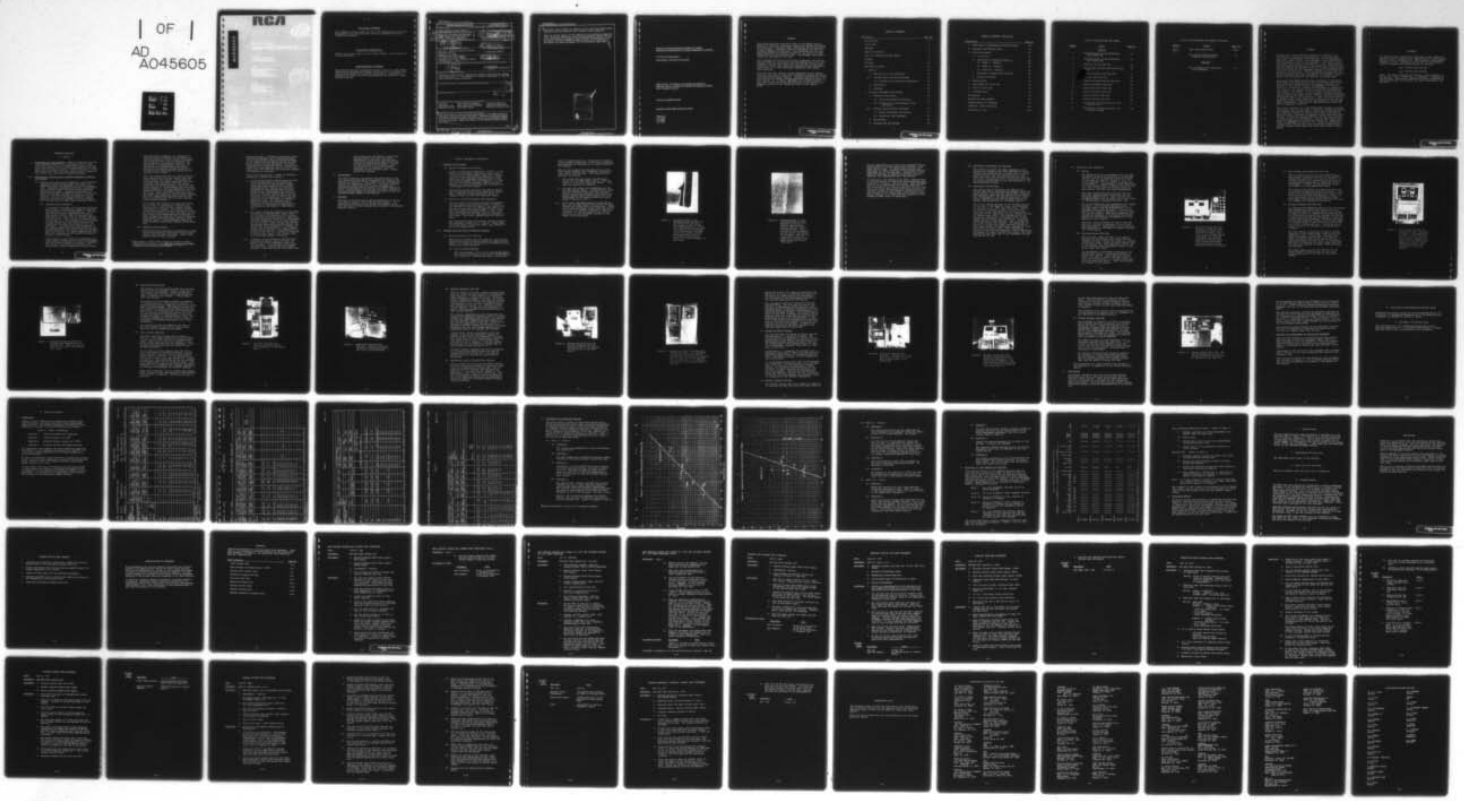

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REPORT DOCUMENTATION PAGE

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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Thyristor	Power Switching Component	Transcalent Thyristor
High Current SCR	Power Conditioning Component	Production Engineering
Heat-Pipe Cooling	Solid State Device	Electrical Testing of SCR

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This third Quarterly Report describes the progress on the MM&TE program for Transcalent (Heat-Pipe cooled) thyristors. Production engineering measures for the device and the pertinent state-of-the-art on the engineering sample devices is included. Actual test results on the engineering sample devices are listed.

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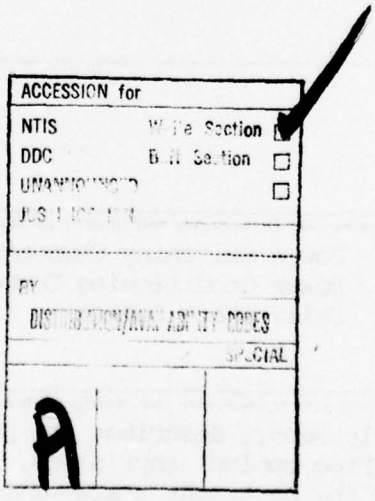
20. The present status includes the completion of the engineering sample device fabrication with the extensive testing sequence nearing completion.

Plans for the next Quarter include completion of the engineering sample devices, electrical, mechanical, thermal and environmental testing; selection of the five samples for shipment to the Government and preparation of the Test Report for these engineering samples, as well as the initiation of the material and parts procurements for the Confirmatory sample phase.



MANUFACTURING METHODS AND TECHNOLOGY (MM&T)
MEASURE FOR FABRICATION OF SILICON TRANSCALENT THYRISTOR

Third Quarterly Progress Report

Period Covered: 1 April 1977 to 30 June 1977

Object of Study: The objective of this manufacturing methods and technology measure is to establish the technology and capability to fabricate Silicon Transcalent Thyristors.

Contract No. DAAB07-76-C-8120

Prepared by:
S. W. Kessler
R. E. Reed
D. R. Trout

ABSTRACT

This third quarterly technical report on the MM&TE Contract DAAK07-76-C-8120 for Transcalent (Heat-Pipe cooled) Thyristors describes the engineering sample fabrication and testing phase of the program. Progress on device refinements for the Confirmatory Samples is described. Also described are the problems encountered and results achieved in the testing of some characteristics for the first time. Sub-assembly fabrication yields are discussed in the text.

Also included are details of the test procedures, the electrical/environmental test results and the photographs of the test equipment that has been built for this program. Actual test results on eleven total engineering devices reveal conformance with almost all of the electrical, mechanical and thermal specifications.

Plans for the next quarter include completion of the fabrication and evaluation of additional engineering sample thyristors, including environmental testing. Selection and delivery of the five engineering samples remains scheduled during the next report period. Dr. R. Eaton, MERADCOM, will witness testing, review test results and guide the selection of the devices for shipment during his next scheduled visit to the vendor's plant.

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PURPOSE

The purpose of this production engineering contract is to establish the technology and capability to fabricate heat-pipe cooled semiconductor power devices, silicon Transcalent Thyristors, Type J-15371. The subsequent pilot production of these devices is a part of the contract. This report covers the efforts performed by the contractor in the third quarterly period to modify the R&D device for production, establish process and fabrication methods as well as to modify and construct the varous types of test equipment required to adequately characterize the thyristor. Plans for future work are also presented, corrective action is delineated for problems that have been encountered and other information is discussed to help assure that the purpose of the contract is accomplished.

This contractual MM&TE program will establish the production techniques, establish quality control procedures and verify a pilot production capability for the J-15371 thyristor, conforming to the drawing attached to AMENDMENT 1 of SCS-477. Electrical, mechanical, thermal and environmental inspections are a part of the program as well as extensive documentation requirements, per DD1423. No high volume production facilities existed at the start of this contract for the Transcalent type of solid-state power device. However, production planning constitutes Step II of the contract. Thus, the time required to produce future large quantities of the J-15371 will be reduced for either current military requirements or future emergency requirements. Reduction of the reproductive costs are also an important objective.

The J-15371 thyristor is a 400 amperes RMS, forced air cooled solid-state power control device, utilizing integral heat-pipes for improved cooling efficiency, lighter weight and smaller size than the conventional devices with their external heat-sinks attached. Improved reliability results from these innovations. A blocking voltage capability of 800 volts minimum at 125^{o} Celsius is a requirement. Original R&D efforts were conducted successfully by RCA under Contract No. DAAK02-69-C-0609, for MERADCOM, Ft. Belvoir, VA. Potential applications include power conditioning, power switching, phase control, voltage variable power supply and motor speed control equipments.

GLOSSARY

All abbreviations, symbols and terms used in this report are consistent with the Electronics Command Technical Requirements SCS-477, dated 5 December 1974. This Technical Requirements document, in turn, references MIL-S-19500 for the abbreviations and symbols used therein except, as follows:

V_{GR} = Reverse Gate Voltage

I_{GR} = Reverse Gate Current

Note: The format used for this report is that specified in the DD 1423, namely, ECIPPR No. 15, Appendix C, augmented by MIL-STD-847A. Sub-section numbering is based on Appendix C and the applicable test methods are those referenced in MIL-STD-750B.

NARRATIVE AND DATA

1. Device

a. Description of the Structure - Refer to pages 9-13 of the First Quarterly Report for a description of the Transcalent Thyristor device, the applicable reports, and the applicable patents as well as the advantages of this heat-pipe cooled technical approach. Refer to Figure 1 in the Second Quarterly Report for the cross-section drawing of the J-15371 with the external dimensions added.

b,c. Defining the Problem Areas and Work Performed to Resolve the Problem

(1) Conversion of Design for Production - The Transcalent thyristor design achieved under R&D Contract No. DAAK02-69-C-0609 was described in the FTR, October, 1972. Subsequent refinements have been incorporated under Contract N62269-73-C-0635 and by RCA-funded engineering projects. Additional engineering is being applied under the MM&TE program to convert the design to one more suitable for production, as described in the First and Second Quarterly Reports covering the period 27 September 1976 to 31 March 1977 and below for the most recent quarterly period.

(a) Improved dv/dt Capability

A refinement described in the previous Quarterly Reports was to increase the number of shorting dots employed in the cathode pattern. The reason for this pattern improvement was that a displacement current flows in the gate layer when there is a rapid rate of change of applied voltage (dv/dt). This current is injected into the cathode layer by the polarity of the applied voltage and may have sufficient energy to unintentionally trigger the thyristor into full conduction. The relatively high resistance of the lightly doped gate layer contributes to the voltage difference that occurs from the displacement current flow. At higher temperatures, this effect is augmented by the thermally generated carriers in the silicon.

A gate layer of lower effective resistance provides greater conductivity for both the displacement and thermal generation currents. Therefore, the thyristor can operate with higher dv/dt values and at higher temperatures without being

unintentionally triggered into conduction.[1] This gate layer resistance can be effectively reduced internally in the silicon by changing the diffusion profile and by shortening the path length for the spurious currents. The shortening is accomplished by the use of a multiplicity of shorting dots that shunt a portion of the spurious currents directly to the metallized cathode/emitter contact on the surface of the silicon.

The first two devices with the larger shorting dots (described in the last report) were fabricated during this period. Preliminary results indicate that these thyristors will have a greater dv/dt capability than any of the previously fabricated devices. One device has a gate current of 78 milliamperes and the other 400 milliamperes. The room temperature blocking currents of the two thyristors are very low, 7 and 25 μA. These very small blocking currents, the higher gate currents, and the larger shorting dots will undoubtedly make these devices less prone to unintentional turn-on with a rapidly rising applied voltage.

The greater gate currents on these new devices are a result of intentionally diffusing the emitters into a base having a greater surface concentration of dopant. The greater surface concentration raises the whole diffusion profile so that the resistance of the gate layer is less. This higher base concentration thus provides a lower voltage drop from the flow of any displacement currents resulting from a rapidly rising forward voltage. The displacement current is also shunted to the emitter through the shorting dots.

(b) Diffused Silicon Wafers

Difficulties were originally encountered in transferring the diffusion technology from the Somerville to the Lancaster locations. These difficulties have now been resolved.

[1]Adolf Herlet & Peter Voss, "State of the Art in Power Semiconductor Devices", 1977 IEEE/IAS International Semiconductor Power Converter Conference, p. 7-24

Progess was made in diffusing acceptable wafers with each successive lot of wafers processed. It was from the most recent Lancaster-diffused lot of wafers that the devices having the best dv/dt capability were fabricated. As further evidence, one of these two devices also had the lowest 800 volts blocking current at both room temperature and 125°C that has ever been recorded on Transcalent thyristors.

During this time period, a number of diffusion engineering problems were solved:

i. The blocking voltage problem resulting from cross-contamination of the dopants was solved by cleaning the furnace's process tubes which were involved in the cross-contamination, by limiting the operations performed in each furnace tube, so that wafers having n-type doping are never processed in the same furnace tube in which the high voltage p-type junctions are diffused and, as a precaution, the n-type deposition furnace was moved to a separate laboratory room. The installation of additional diffusion furnaces is being completed to facilitate the separation of the operations performed in each furnace tube.

ii. The voltage blocking capability of one group of wafers was degraded when chips formed in the silicon at the boundary of the oxide/poly-crystalline silicon layers. This chipping was apparently caused by the differences in thermal expansion of the silicon dioxide and the silicon. After etching the insulating pattern and metallizing the wafers, the stress from these differences in thermal expansion was concentrated at a step created by the etching process. The problem was corrected on the next lot of wafers by applying a thinner oxide layer. This thinner layer still provides adequate insulation.

iii. In another lot of wafers the emitters were diffused too deeply, making the gain too great in the N-P-N transistor section of the thyristor. This excessive gain caused the thyristors to break over and conduct current at less than the 800 volts specified.

This problem was corrected by instituting greater control over the V/I control measurement at the wafer thinning operation and by favoring the lower end of the allowed resistance distribution. Diffusing the emitters into a higher surface concentration also permits a greater tolerance in the diffusion time. Yields should thus improve.

d. Conclusions

The device component refinements described above, along with the design refinements incorporated or planned, are expected to produce a J-15371 device to meet the specifidations and inspections of SCS-477. The wafer diffusion transition difficulties have now been resolved and Lancaster-diffused wafers conform to the MM&TE specifications. Unfortunately, much of the time delay incurred on the engineering samples is expected to impact on the confirmatory sample phase of the contract.

e. Drawings

Drawings of the piece parts and sub-assemblies of the device were included in the First Quarterly Report. All engineering drawings for the device were brought up to date and these revised drawings were included in the Second Quarterly Report.

2. Process, Equipment and Tooling

a. Purpose of Each Step

(1) Device Processing and Tooling

Figure 4, Engineering Drawing No. 3025577, in the First Quarterly Report showed the flow of parts through the various assembly steps and a descriptive title was listed for each operation. Also shown were the subassembly drawings and the fixture drawing numbers for each operation. In both the First and Second Quarterly Reports the procedures for using the fixtures were included with a photograph of each fixture.

Flow process cards continue to be used to record and control the flow of parts through the laboratory. Examples of these cards were shown in Figures 5 and 6 of the First Quarterly Report.

(2) Electrical and Environmental Test Equipment

The flow chart of the electrical and environmental testing sequence was given in Figure 7, Drawing No. 3025578, of the First Report. The name of the test was given as well as the special conditions and the MIL-STD-750B method number. Also, listed were the sampling percentages for the pilot run. Long time tests had the time interval indicated in the figure. This chart remains valid for the program.

Test Data Record Forms with actual results recorded are included in Table 1a, b, c and d. These forms are being used to record the actual test results on all of the sample units.

b,c. Problem Areas and Work to Resolve Problems

(1) Device Processing and Tooling

Fabrication processes that are known to limit the production quantities are being improved by improving the yields, by increasing the quantity per operation and by reducing the labor required.

(a) Heat-Pipe Sub-Assembly

The fixtures shown in Fig. 4-7 of the Second Report were used to fabricate the heat-pipe sub-assemblies for 16 devices. Records were kept to verify the

yield of these operations. There were 27 vacuum-tight assemblies among the 32 heat-pipe assemblies. One heat-pipe was repaired for an overall yield of 87.5 percent.

Most of the failures were detected prior to the final device assembly and, therefore, represented only a small loss of parts. The failures were analyzed, as follows:

i. One vacuum leak was between the Wolverine tubing and the OFHC copper tubing. Refer to Figure 2 in the First Quarterly Report. This leak was repaired by rebrazing.

ii. One leak was between the molybdenum disc and the OFHC copper tubing. A metallurgical cross-section was made of the leak area and there were no voids large enough at the section nor cracks observed which could explain the leak. Photographs of the cross-sections are reproduced in Figures 1 and 2.

iii. Three leaks developed between the molybdenum disc and the OFHC copper tubing after the weld flanges were brazed onto the heat-pipes. These joints were previously vacuum tight and did not leak until the residual stresses in them were reversed to a tensile stress by the wicking operation and the subsequent brazing of the flange to the heat-pipe.

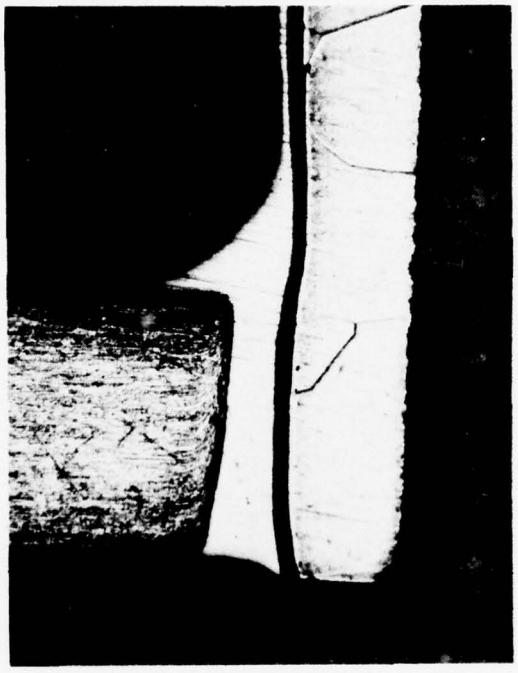


Figure 1. Photomicrograph of the molybdenum disc brazed into the end of the heat-pipe. 48 X magnification is used. The molybdenum disc is on the left side of the photograph. This cross-section was made in the area where a vacuum leak was detected with a helium mass spectrometer. There are no voids evident in the braze.

Figure 2. Photomicrograph of the molybdenum disc to braze material interface at a greater magnification (600 X) than the Figure 1 microphotograph. The plating on the molybdenum can be seen in the center of the photo. The curving lines result from the shearing of the disc from sheet stock during parts fabrication.

Another subassembly was lost by the molybdenum button being cocked at a slight angle after brazing. This joint did not leak. It should also be noted that there were no leaks occurring at the ceramic-to-metal interfaces nor at the end caps. Ceramic and end cap leaks had occurred in making earlier heat-pipe assemblies, but improvements were incorporated.

In conclusion, the results of iii, above, indicate that it would be better to leak check the molybdenum/copper braze joint of Figure 1 after wicking. This procedure should be followed because the wicking operation is not considered to be a brazing operation but the wicking is the first temperature cycle which reverses the residual stresses in the copper to molybdenum joint. Leak testing of the flange joints will continue after brazing because it is then that the integrity of the ceramic-to-metal seals is determined.

(b) Contouring and Etching of the Chip

This effort to reduce the labor required in contouring and etching of the chip involved the specification and ordering both a special pair of pliers having parallel jaws and a new teflon seal ring. When these parts are received they will be used to construct a new masking tool in which the wafers can be inserted faster than in the tool described in the Second Quarterly Report.

(c) Passivation of the Chip

The coating used to passivate the edges of the silicon chip after contouring was changed during the report period. The previous coating was a flexible, two component system and was used on devices Serial Nos. N1 through N9. The newer coating is a rigid, single component system that had been used on all devices fabricated prior to the MM&TE contract.

The initial change was made to the flexible coating at the start of the MM&T to reduce the likelihood of cracking at the -25°C test conditions. However, the blocking voltages of three of the first engineering samples degraded when the devices were subjected to the temperature cycling, thermal fatigue or thermal shock tests. This degradation of the voltage was suspected to be caused by the coating change and the process has returned to the proven rigid coating on later devices. Also, a sample of the rigid coating was retested. The sample was applied to a silicon test wafer and after curing it was cycled between the temperature extremes of -25°C and +125°C for eight times. After temperature cycling the coating was examined on the metallurgical microscope for cracks and none were found. The rigid coating has thus been used on all subsequent devices from Serial No. N10.

(2) Electrical Test Equipment

(a) Status

The remaining two test equipments have now been assembled, modified and checked out as required for the total of 41 different electrical tests (13 methods) for SCS-477, Tables I, II & III, dated 5 December 1974 as amended 31 August 1976 by Amendment 1. Approximately a dozen mechanical and environmental tests in SCS-477 bring the overall total to more than 50 different tests for each device, including the final measurements.

The surge current and turn-off time test sets have been completed and utilized for the Engineering Sample devices. Both test sets will be demonstrated to Dr. R. Eaton on his next visit to RCA-Lancaster, scheduled for July, 1977.

All of the electrical test equipments were listed in Table 1 of the Second Quarterly Report. In the same report, the tests performed in each equipment were listed in Table 2. Actual test results are listed in Section 5, "Data and Analysis" of this report. Some test procedures were included in Appendix C of the Second Quarterly Report and the remaining procedures are in the Appendix of this report.

Functional block diagrams for each of the test sets were included in Appendix C of the First Quarterly Report. Photographs of the electrical test equipment are included in Figures 3 through 12 of this report.

(b) Blocking Current Test Set

This test set, shown in Figure 3, is used to measure both the forward and reverse blocking (leakage) currents at the full rated a.c. voltage of 800 volts peak. These off-state currents can be measured at both room temperature (25°C) and at the maximum rated temperature (125°C) of the Device Under Test (DUT).

The measurement is performed by monitoring the voltage drop across a calibrated resistor in series with the DUT. This enables an oscilloscope to be used to measure the peak current since the oscilloscope is a voltage rather than a current measuring device. Ohm's law converts the reading to the current.

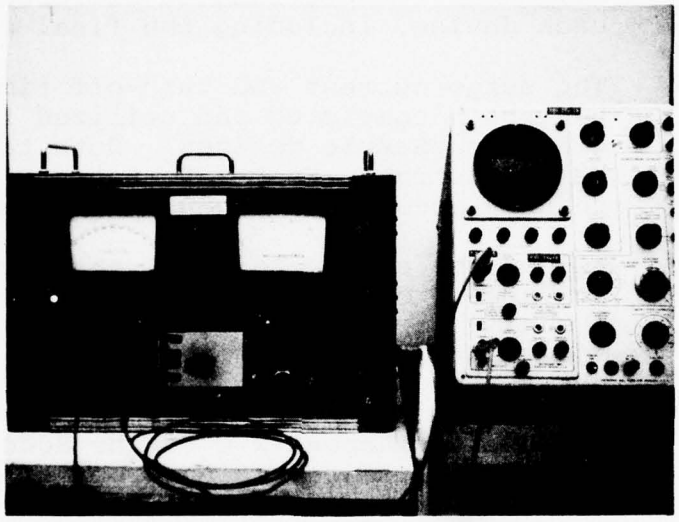


Figure 3. Blocking Current Test Set. This set is used at room temperature as well as in conjunction with an oven (Fig. 5) or a vacuum system (not shown) for the high temperature and reduced barometric pressure tests. Both forward and reverse blocking currents can be measured with this equipment.

(c) Gate Trigger Characteristics Test Set

Figure 4 shows the test set for measuring the D.C. Gate Trigger voltage and current at the various temperatures specified (-25, +25 and +125°C). It is small enough to be transported to the oven or environmental chamber used to establish the test temperature. A socket is also provided inside the cabinet for room temperature tests.

Both forward and reverse gate characteristics can be measured by changing one polarity switch. Two ranges are provided with meters for devices having both low and high gate characteristic values. A reset push button switch is provided to facilitate repeat readings for better accuracy after the DUT triggers into conduction (on-state).

(d) Blocking Voltage Life Test Set

The test set for performing the long time (500 hours), high temperature (125°C) life test at full a.c. rated voltage (800 volts peak forward and reverse) is shown in Figure 5. Meters are provided for the DUT temperature, elapsed time, voltage and current. A jack is provided for the measurement of the peak voltage with an oscilloscope. Indicator lamps and high voltage fuses are included in the power supply to indicate whether a DUT has failed to block the high voltage during the tests. Provisions are included for up to six devices to be tested simultaneously.

The power supply is connected through a voltage regulator to the primary power lines of the high temperature oven. In this way, the power and timing is removed from the DUT in the event of a power interruption that would reduce the oven temperature below the test value. An interlocked oven door also removes the high voltage from the DUT when the oven door is opened, thus protecting the personnel.

This power supply can also be used for the Reduced Barometric Pressure test for full wave voltage application to the DUT in the vacuum chamber.

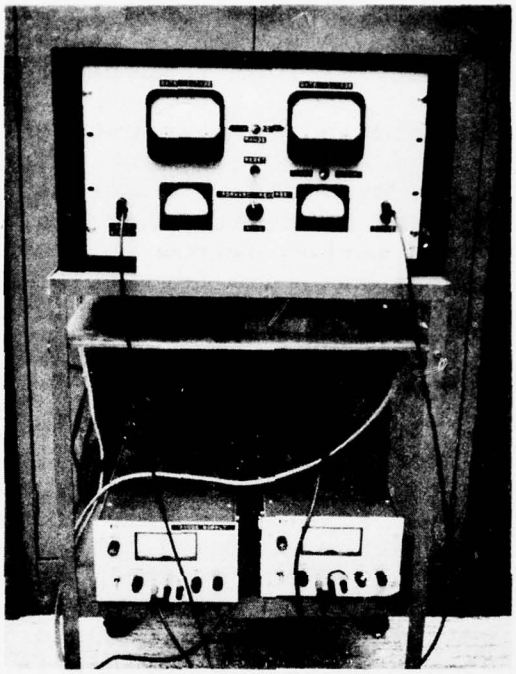


Figure 4. Gate Trigger Voltage and Current Test Set. This set is used at room temperature as well as in conjunction with an oven (Fig. 5) or an environmental chamber (not shown) for the high and low temperature tests. Both forward and reverse gate characteristics can be measured.

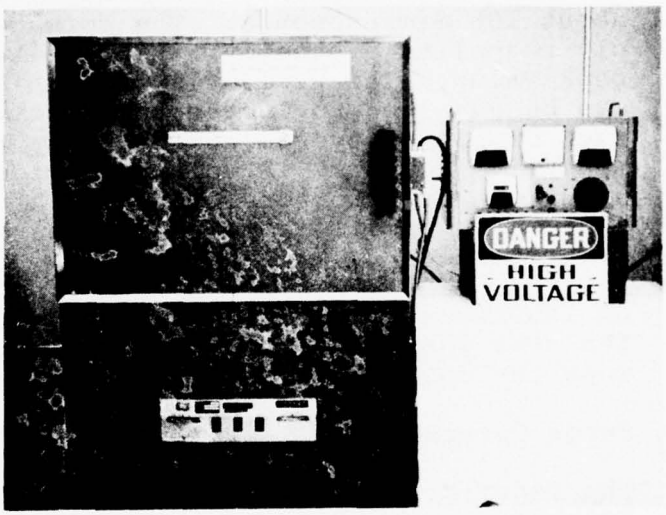


Figure 5. Blocking Voltage Life Test Set, including the temperature controlled oven. This oven is also used for the other high temperature tests.

(e) Turn-Off Time Test Set

See Figure 6 for this sophisticated test set that applies three independent voltages to the DUT in the correct time sequence. Three synchronized pulse generators with adjustable time delays are used to sequence the voltages. A 60 Hz repetition rate is used.

The on-state current supply provides 100 amperes of forward current to fully turn-on the DUT. A reverse current supply commutates the DUT off after about 100 microseconds. The forward voltage supply reapplies a steeply rising voltage of the full peak value. The time delay for this reapplication can be adjusted to locate the interval at which the DUT has recovered sufficiently to block the reapplied voltage. A voltage divider (100:1) and a current transformer (0.5 V/1.0 A) are used to facilitate oscilloscope monitoring of all three parameters.

An interlock is used for safety on the door of the test chamber to turn-off the high voltage when the door is opened for any reason.

(f) Surge Current Test Set

The repetitive surge current test is shown in Figure 7. Three power supplies are also involved in this test of DUT's ability to withstand overloads. Sequencing on the exact one-half or full 60 Hz cycle is designed into the equipment. High voltage interlocks are used for safety of the operating personnel.

An a.c. heating current supply heats the DUT to its normal operating temperature before a second supply applies a single, one-half cycle forward current surge to the DUT. On the subsequent one-half cycle, an 800 volts peak reverse a.c. voltage is applied to test whether the device has retained its blocking capability following the surge. This surge sequence is repeated ten times at one minute intervals. All parameters are recorded temporarily on a storage oscilloscope for accurate readings.

Other test conditions, such as, higher peak surges, lower reverse voltages and different time intervals can be set-up, if desired. Forced air cooling is utilized.

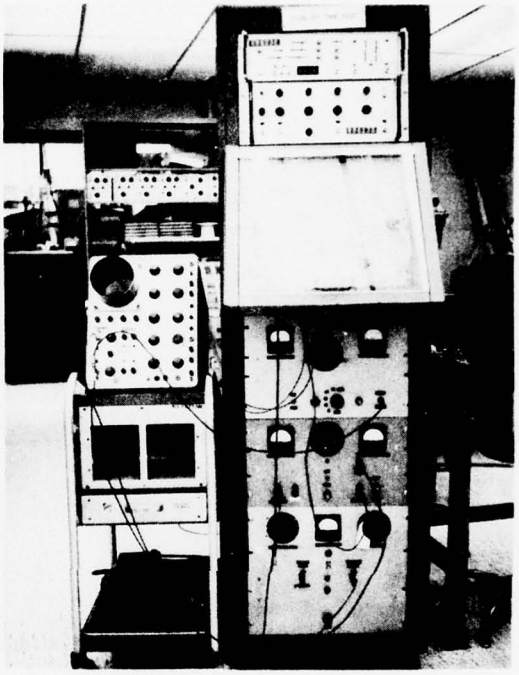


Figure 6. Turn-Off Time Test Set. The DUT is mounted inside the transparent, interlocked door.

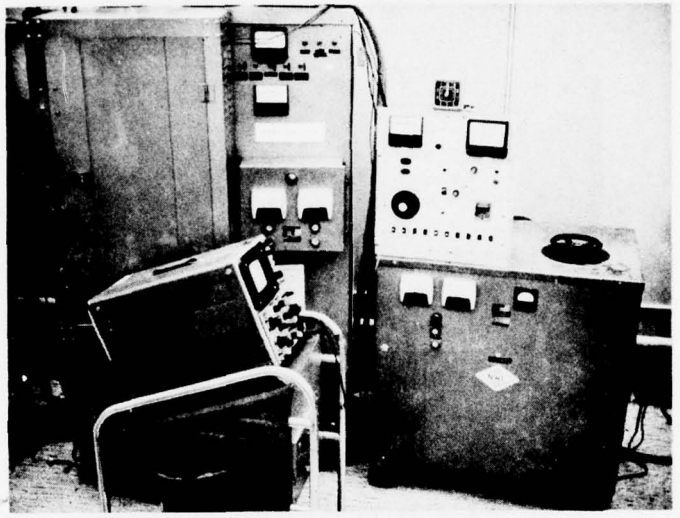


Figure 7. Repetitive Surge Current Test Set. The DUT is mounted inside the interlocked door on the left in the photograph.

(g) Thermal Impedance Test Set

Refer to Figure 8 for this, another sophisticated test set involving three separate time sequenced, power supplies. A high current D.C. supply applies the heating current to the DUT. A reverse current commutating supply interrupts the heating current briefly (0.2-0.5 ms) but repetitively for a measurement of the junction temperature dependant forward voltage at a d.c. metering current of four amperes. A type W plug-in amplifier is used in the oscilloscope for improved accuracy of this voltage reading.

The junction temperature is then determined from a previously measured calibration curve of forward voltage vs. temperature for the DUT. The ambient air and heat-pipe temperatures are measured as well as the input power to the DUT. These values are used to calculate the thermal resistance values of the DUT. Forced air cooling is utilized throughout the test and thermal equilibrium is established before the readings are recorded.

A shunt diode circuit is utilized in the test circuit to bypass the hundreds of amperes of heating current during the commutation interval. This shunt minimizes the unmanageable transients that would occur if such a high current were switched off and on abruptly. The high forward voltage drop of the diodes used causes them to stop conduction when the DUT is "on."

Transient thermal impedance can also be measured if a suitable high speed recorder is used in conjunction with this test set. The heating current level and cooling air flow rates are adjustable.

(h) Exponential Rate of Voltage Rise (dv/dt)

Figure 9 shows the dv/dt test set which consists of a high voltage RC network for charging a capacitor at an exponential voltage rate. The exponential rate is variable (by adjusting the value of R). The peak applied voltage is also adjustable to any value up to 1,000 volts. The DUT is connected in parallel with the capacitor (in a non-conducting state) and the exponential voltage is applied to the DUT through a current limiting resistor.

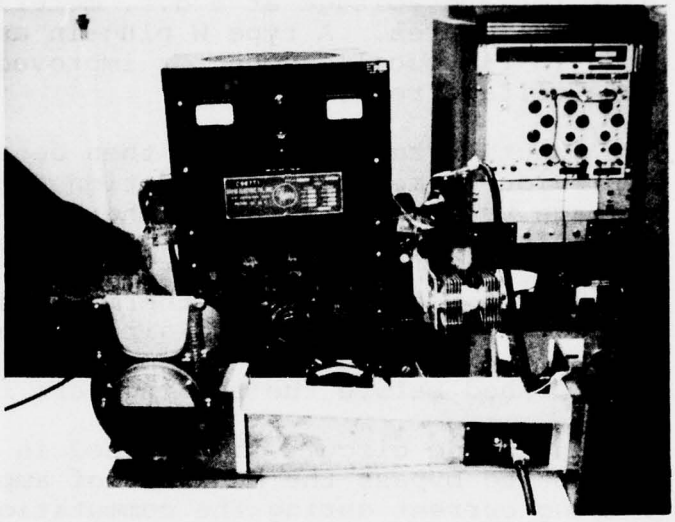


Figure 8. Thermal Impedance Test Set. The DUT is mounted in the right-hand end of the cooling air duct shown in the foreground.

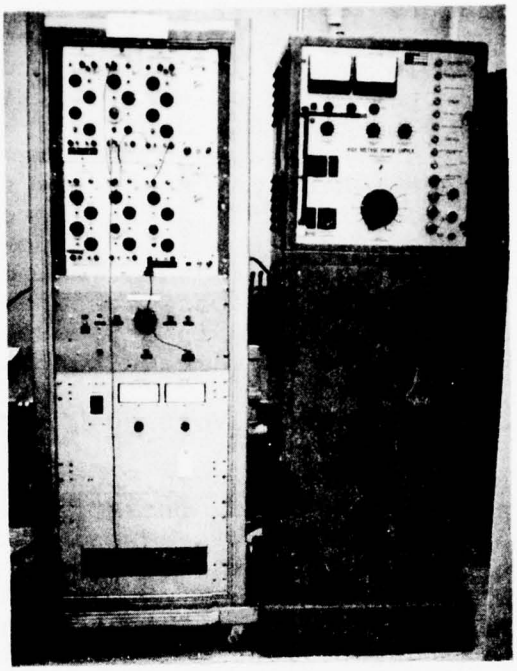


Figure 9. Exponential Rate of Voltage Rise (dv/dt) Test Set. This equipment is used in conjunction with an oscilloscope (not shown) to measure the rise time of the voltage and with an oven (Fig. 5) to achieve the specified high temperature for the DUT.

Faster and faster rise times are applied to the DUT until the value is determined at which the DUT begins to conduct due to the spontaneous turn-on caused by the displacement currents in the internal capacitance of the device.

This equipment contains a socket for room temperature tests. The test set can also be connected to a temperature controlled oven, with suitable safety interlocks, to measure the dv/dt characteristics at elevated temperatures, as required by the MM&T contract. An oscilloscope is used in every case to measure the steeply rising waveform which may reach the specified voltage measurement point in two microseconds, or less. A 20 to 60 Hz repetitive exponential waveform is used to facilitate the viewing of this very fast transient on the oscilloscope. A hooded kinescope is required in any case, because of the very dim, fast trace on the screen.

(i) Forward On-State Voltage

The test set shown in Figure 10 applies the full rated average a.c. current to the DUT. The cooling air flow is adjusted to achieve the required 100°C on the case of the heat-pipe of the DUT before the peak forward voltage is read on the oscilloscope. This reading cannot be taken on a conventional voltmeter since the a.c. waveform is distorted.

Synchronous a.c. triggering is utilized at an adjustable amplitude to assure that the specified minimum conduction angle is achieved during the test. The conduction angle is also displayed on the oscilloscope.

It is convenient during this test to also measure the temperature at several points along the heat-pipes. In this way, the heat-pipes' thermal balance and isothermal characteristics can be verified. A poorly functioning heat-pipe will not be isothermal. Properly functioning heat-pipes are important not only for the reliability of the DUT, but also because the on-state voltage is a function of the junction temperature.

(j) Holding Current Test Set

The holding current test set is shown in Figure 11. It utilizes the same anode and gate power supplies

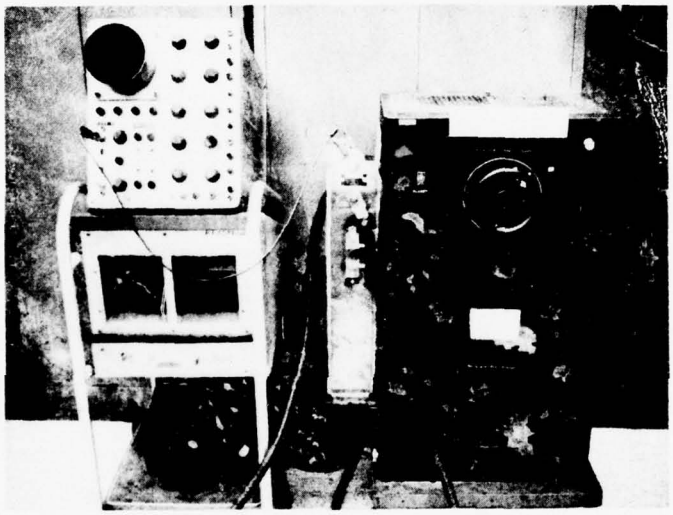


Figure 10. Forward On-State Voltage Test Set. The DUT is mounted at the top of the cooling air duct in the center of the photograph.

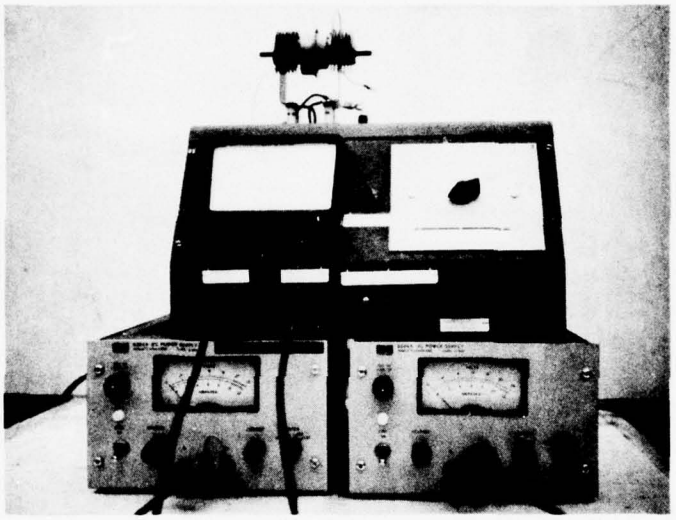


Figure 11. Holding Current Test Set. The DUT is mounted on the stand-off insulators at the top of the photograph. The Power Supplies shown are also used for the Gate Characteristics Tests (Fig. 4).

as the Gate characteristics test set described above. After the DUT is triggered into full conduction, the gate trigger voltage is removed and a series resistor is used to reduce the on-state current to the point at which the DUT ceases to conduct.

This equipment could also be used to determine the latching current of the DUT, but this parameter is not specified in the MM&T contract.

(k) Thermal Fatigue Test Set

The equipment in Figure 12 is used to repeatedly cycle the DUT from the on-state at full current to the off-state. Forced air cooling flow is adjustable to assure that the specified minimum and maximum temperatures are achieved on every cycle. This temperature excursion is recorded for as many as two DUTs at a time. The recorded charts verify not only the temperature range but also the number of cycles operated.

The number of cycles is also adjustable with an automatic shut-off after the last cycle. A continuous run switch is provided for long term cycle life test position and the current through each of the inverse parallel connected DUTs is independently adjustable.

The control, monitoring and interlock features are automatic to permit unattended operation. The gate trigger voltages have a phase adjustment to permit optimizing the conduction angle when each new device is set-up for test.

Test procedures for these quipments are included in the Appendix or in Appendix C of the Second Quarterly Report.

d. Conclusions

The process, equipment and tooling have been designed, fabricated and used to fabricate and evaluate the engineering sample devices. More devices were fabricated than will be shipped in fulfillment of the Engineering Sample requirement. This approach enabled a wider variety of process changes and device characteristics to be evaluated.

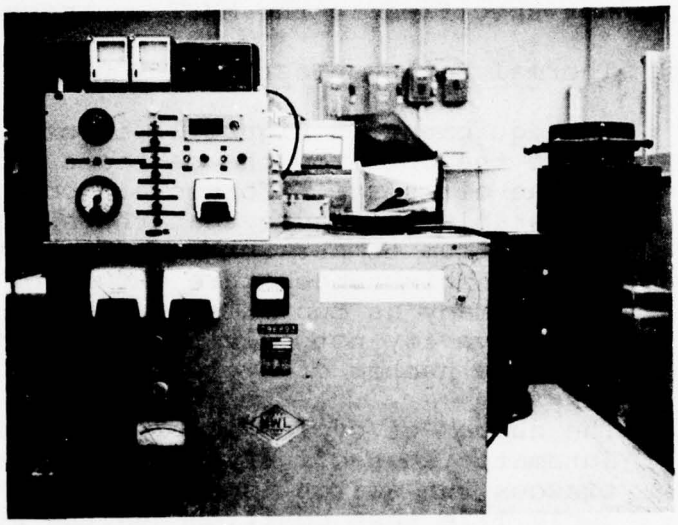


Figure 12. Thermal Fatigue Test Set. The DUT is mounted out of view in the end of the air cooling duct at the back of the test set.

The through-put of some of the equipment will be increased in the confirmatory sample phase to facilitate the larger pilot run. Yields have been improved where high scrap was produced, such as, in the heat-pipe sub-assembly described above.

The modified processes, tooling and equipment described in this and the prior reports have succeeded in producing and are evaluating the engineering sample devices in accordance with SCS-477 and paragraph F.47. This evaluation is expected to be completed in the next report period. Any additional limitations that become evident will be corrected in the confirmatory sample phase.

Quotations are being obtained for the additional fixtures that will be necessary to fabricate the larger quantity of pilot run samples under this contract.

e. Drawings and Photographs of Tooling and Equipment

Copies of the drawings of the special tools and fixtures were included in the First Quarterly Report along with Block Diagrams of the test equipment. Tools and fixtures that were revised were included in the Second Quarterly Report. Photographs of these items were included in both reports.

Photographs of the electrical test equipment were included above, adjacent to the text references that describe each equipment item.

Some testing procedures for the electrical test equipment were included in Appendix C of the Second Quarterly Report. The remaining procedures are included in the Appendix of this report.

3. Flow Chart of Manufacturing Process Yield

Manufacturing process yields are to be determined during the Pilot Run. A preliminary determination on the heat-pipe subassemblies is reported in Section 2, above.

4. Equipment and Tooling Costs

This information is not included since such data is not generally applicable to a Firm Fixed Price Contract on equipment and tooling that is furnished by the contractor.

5. Data and Analysis

a. Inspections

Group A, B and C Inspections as specified in SCS-477 were continued during the report period on eleven engineering sample devices. The minimum acceptance criteria are those specified in Section F.47 of the contract, as follows:

TABLE I - GROUP A INSPECTION

Subgroup 1	Visual and Mechanical Inspection
Subgroup 2	Forward Blocking (at 25°C)
Subgroup 3	Forward Blocking Current (at 125°C)
Subgroup 4	On-State Voltage and Holding Current

All engineering test samples are being tested for compliance with Section 3 in accordance with Section 4 of SCS-477. In a few cases, sample quantities will be tested rather than all eleven devices.

To date, all mechanical; most electrical, thermal and environmental tests have been completed on several of the initial devices. Actual results are listed on the Test Data Record Forms, Table 1a, b, c & d.

In many cases, additional engineering data has been secured to guide production controls and process refinements to be incorporated in the subsequent Confirmatory Sample and Pilot Run Phases. All testing will be completed in July and possibly August on the Engineering Sample devices.

Table 1a. Test Data Record Forms

ITEM: SILICON TRANSCALENT THYRISTOR, J15371 CONTRACT: DAA B07-76-C-8120

SPEC: SCS-477 5 DECEMBER 1974 & MFR: RCA (EO&D) LANCASTER, PA.

AMENDMENT - 1 31 AUGUST 1976 BUYER: COMM.SYS.PROCUREMENT BRANCH (USAECOM),FT.MONMOUTH,N.J

GROUP	A											
SUBGROUP	1	2	2	4	4	4	3	3	3	3	4	4
NO.UNITS TESTED	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
TEST	Visual & Mech.	Reverse Current	Forward Blocking	Gate Trig.V	Gate Trig.I	Holding Current	Reverse Current	Forward Block'g	Gate Trig.V	Exp.Rate V Rise	Turn-off Time	On State Voltage
MIL-STD-750 METHOD	2071	4211	4206	4221	4221	4201	4211	4206	4221	4231	4224	4226
TEST CONDITION	Visual Inspt.	25°C →				→	125°C →		→	→	25°C →	
SYMBOL	-	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	I_H	i_{RBOM}	i_{FBOM}	V_{GT}	dv/dt	t off	V_{FM}
MAX.	-	15mA	15mA	5Vdc	500mAdc	500mAdc	60mA	60mA	5.0Vdc		150µs	2.0V
MIN.	-									200V/µs		
1st Qtr., 1977 Date Tested UNIT NO.	A R C E C J											
N1	✓	0.3	0.4	1.1	545	4	53	75	0.5		34	1.3
N2	✓	0.2	0.3	1.1	620	4	40	>72	0.5	50*	36	1.3
N3	✓	0.3	0.3	1.0	535	4	70	>64	0.5	152*	32	1.2
N4	✓	0.2	0.2	0.6	23	12	5	6 Δ	0.3	1*	68	1.4
N5	✓	0.2	0.2	0.7	53	9	5	10	0.3	3*	46	1.5
N6	✓	0.2	0.2	0.6	30	9	3	6	0.3	1*	48	1.5
N7	✓	0.2	0.2	0.6	73	14	3	6	0.3	5*	73	1.6
N8	✓	2.7	0.3	0.6	30	9	12	13 Δ	0.3	28*	54	1.4
N9	✓	0.3	0.5	0.6	40	1	3	4 ΔΔ	0.2	14*	90	1.2
N10	✓	0.3	0.5	1.1	160	8	28	41	0.5	190*	36	1.3
N11	✓	2.0	0.6	0.8	50	6	25	37 Δ	0.4	55*	38	1.4

*Test performed at $T_A = 125 \pm 3^{0}_{-0}$°C, gate condition D, but with reduced voltage on some devices. Values with gate condition B were much higher.

Note: Details of test conditions are given in spec.

ΔΔGate Condition A ΔGate Condition B

Table 1b

CONTR'S. TYPE: J15371 DATE TEST COMPLETED: SAMPLE NOS. Page 2 of 4

MFR'S. TYPE: J15371 DATE TEST BEGUN: February, 1977 FR. N1 TO N11

B

1	1. Final Measurements			2			3. Final Meas.		4. Final Measurements				
10%	10%	10%	10%	100%	100%	100%	10%	10%	10%	10%	10%	10%	
Surge Current	Reverse Current	Forward Block'g	Rev. Gate Current	Gate Trig. V	Gate Trig. I	On-state Volt.	Temp. Moist	Cycle & Resist	Blocking per para.	Voltage 4.6.1	Life	Test	
4066	4211	4206	4219	4221	4221	4226	1051	1021	4211	4206	4211	4206	
25°C	25°C →			-25°C →			4211	4206 →	25°C →		125°C →		{case temp, T_C
I_{FM}	i_{RBOM} 15mA	i_{FBOM} 15mA	I_{GR} 1.0Adc	V_{GT} 10Vdc	I_{GT} 1000 mAdc	V_{FM} 2.3V	i_{RBOM} 15mA	i_{FBOM} 15mA	i_{RBOM} 15mA	i_{FBOM} 15mA	i_{RBOM} 60mA	i_{FBOM} 60mA	
10 Surges													
N1	20.6**	51.5**	0.5	1.3	760	1.5	0.2**	0.2**					
N2	0.2	0.3	2.2	1.4	880	1.7	0.2	0.3					
N3	20.6**	4.1**	2.5	1.3	720	1.5	41.2**	10.3**					
~~N4~~	~~0.2~~	~~0.2~~	~~0.2~~	~~0.7~~	~~40~~	~~1.4~~	0.2	0.2					
N5	0.2	0.2	0.4	0.8	70	1.4	0.2	0.2					
N6	0.4	0.3	0.2	0.7	40	1.5	<0.1	<0.1	0.2	0.2	3	6Δ	
N7	0.2	0.3	0.5	0.8	90	1.6	0.4	0.2					
N8	3.7	0.2	0.2	0.8	50	1.4	3.3	0.2					
N9	0.3	0.5	0.3	0.7	50	1.1	0.2	0.5					
N10	0.3	0.6	0.8	1.2	250	1.3	<0.1	<0.1					
N11	2.1	0.9	0.3	1.1	90	1.3	2.1	0.9					

**Device degraded in blocking voltage on another test, but no further degradation occurred on this test.
ΔGate Condition B

GROUP	C									
SUBGROUP	1					2.Final Measurements				
NO.UNITS TESTED	100%	100%	100%	100%	100%	10%	10%	10%	10%	10%
TEST	Physical Dimens.					Shock,	Vibration,	Constant	Accel.	
MIL-STD-750 METHOD	2066					2016	2056	2006		
TEST CONDITION	Figure 1					4211	4206	4221	4221	4226
SYMBOL	A	B	C	D	E	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}
MAX.	5.00"	3.475"	0.700"	1.857"		20mA	20mA	5Vdc	500mAdc	2.5V
MIN.		3.425"	0.600"		6.00"					
UNIT NO.						(Values after Shock and Vibration)		For information only - Not a spec. requirement		
N1	4.81	3.468	0.668	1.815	8.75	41.2**	3.6**	(Can't trigger gate)**		
N2	4.76	3.442	0.669	1.821	8.75	0.3	0.3	1.0	400	1.4
N3	4.80	3.470	0.677	1.807	8.75	268**	18.6**	(Can't trigger gate)**		
N4						0.2	0.2	0.6	30	1.3
N5						0.2	0.3	0.6	50	1.4
N6						0.2	0.2	0.6	20	1.6
N7	4.68	3.423	0.627	1.819	7.25	0.2	28.9**	0.7	60	1.7
N8						3.2	0.2	0.6	30	1.4
N9						0.2	0.4	0.6	30	1.2
N10						0.2	0.4	0.9	160	1.4
N11						1.9	1.4	0.8	50	1.4

**Device degraded in blocking voltage on another test, but no further degradation occurred on this test.

Table 1d

	3.Final Measurements					4.Final Measurements					5	
	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	100%	
	Reduced Barometric Pressure					Salt Atmosphere, Thermal Fatig.					Thermal Resistance	
	1001					1041	para.	4.6.2			3151	
	4211	4206	4221	4221	4226	4211	4206	4221	4221	4226		
	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	i_{RBOM}	i_{FBOM}	V_{GT}	I_{GT}	V_{FM}	θ_{J-c}	
	20mA	20mA	5Vdc	500mAdc	2.5V	20mA	20mA	5Vdc	500mAdc	2.5V	0.15°C/Watt	
											Initial	After -25°C
1	11.3**	67.0**	0.8	140	1.4	26.8Δ	30.9Δ	0.9Δ	140Δ	1.3Δ	0.19	0.39
2	0.2	0.3	1.1	640	1.4	0.3Δ	0.3Δ	1.1Δ	640Δ	1.4Δ	0.14	0.12
3	--	--	--	--	--	28.9Δ	10Δ	1.1Δ	550Δ	1.4Δ	0.15	0.12
4	0.2	0.2	0.6	30	1.5	0.2	0.2	0.6	20	1.4	0.08	0.12
5	0.2	0.2	0.6	50	1.6	0.3Δ	0.3Δ	0.6Δ	45Δ	1.4Δ	0.13	0.12
6	0.2	0.2	0.6	20	1.6	0.1Δ	0.2Δ	0.6Δ	22Δ	1.4Δ	0.16	0.15
7	0.2	45**	0.7	70	1.6	0.5Δ	>20Δ	0.7Δ	70Δ	1.6Δ	0.14	0.15
8	3.3	0.2	0.6	30	1.4						0.11	0.12
9	0.2	0.5	0.6	30	1.2						0.11	0.11
10	0.2	0.5	0.9	160	1.4						0.08	0.09
11	1.9	0.7	0.8	50	1.3						0.09	0.08

Following >200 cycles Thermal Fatigue Test

b. Discussion of Inspection Results

The test results, to date, on the eleven devices built during the engineering phase reveal an obvious consistency or reproducibility of most of the electrical, mechanical and thermal characteristics as well as a general ability to withstand the environmental conditions. Specific comments, analysis and discussion of the test results are listed below by inspection subgroup in SCS-477. Refer to Table 1a, b, c and d for both the specifications (spec.) and the actual measured values.

(1) Table I - Group A

(a) Subgroup 1

All devices are acceptable at Visual and Mechanical inspection.[@]

(b) Subgroup 2

The room temperature forward[@] and reverse leakage currents at 800 volts are well within the spec.

(c) Subgroup 3

Improvement in the forward[@] and reverse leakage current characteristics has obviously occurred at 125°C. The gate voltages are well within spec. and the dv/dt at the high temperature of 125°C is obviously an area for further improvement efforts.

(d) Subgroup 4

The gate voltage, holding current[@] and on-state voltage[@] are all in spec. The gate current on later devices shows considerable improvement. The turn-off time test set was recently completed and used for measurements of the turn-off time parameter on all of the devices. All are in spec.

There is good correlation between the holding current, I_H, and both the Turn-off time and the on-state Voltage Drop. Refer to Figures 13 and 14.

[@]Minimum acceptance criteria for engineering samples.

Figure 13. Correlation of Holding Current and Turn-Off Time

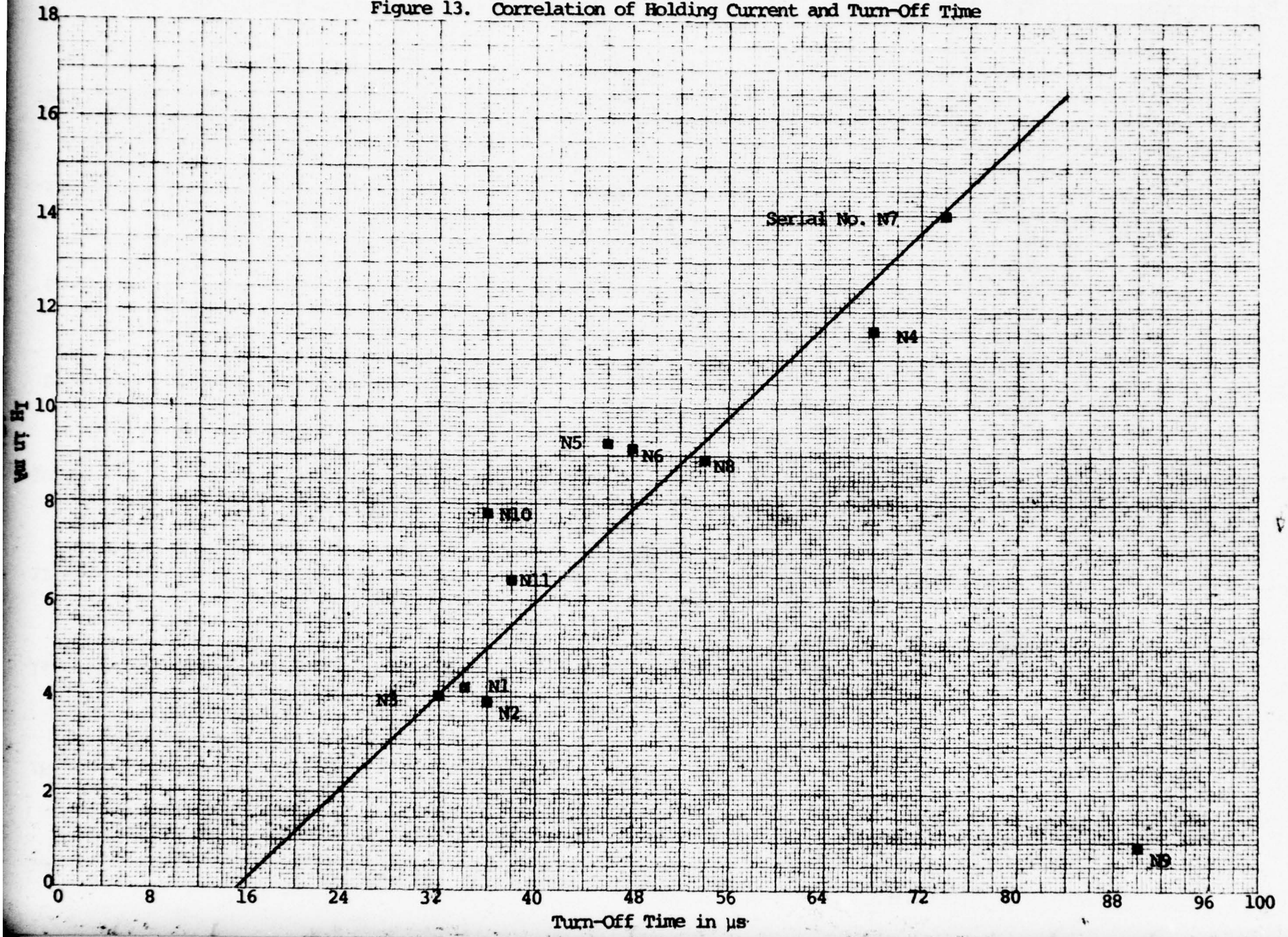
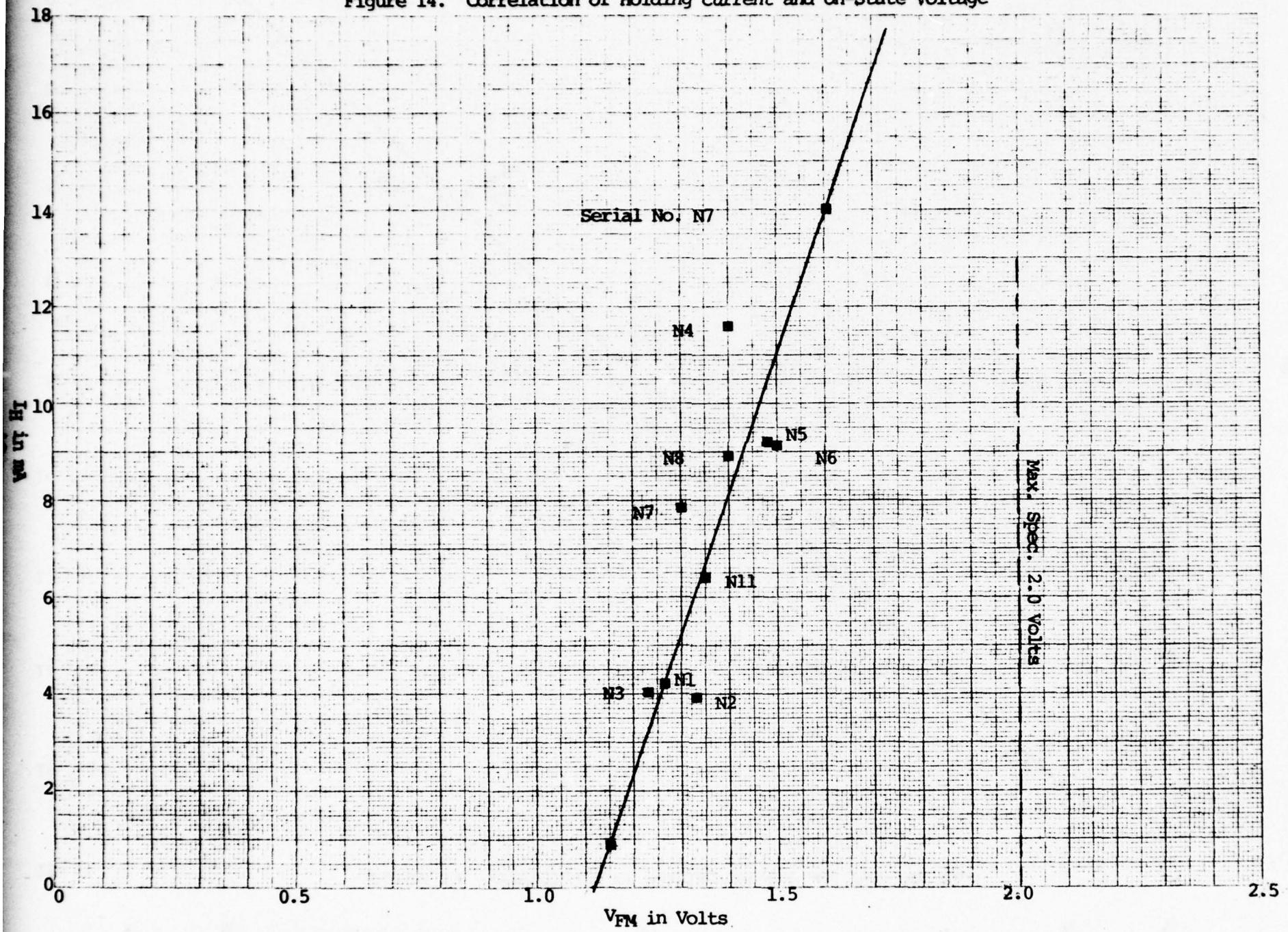


Figure 14. Correlation of Holding Current and On-State Voltage



(2) Table II - Group B

(a) Subgroup 1

The surge current test set was completed and used to measure this parameter during the report period on all eleven devices. All passed.

(b) Subgroup 2

All test results at 25 degrees C below zero were in spec. In addition, the thermal resistance was measured on all devices to detect any hidden damage that might have been caused by the frozen starts. Ten of the eleven devices tested showed no damage (refer to Table 1d). The first had its blocking voltage as well as its thermal resistance degraded by this test.

(c) Subgroup 3

These environmental tests were performed for the first time during the report period. No degradation occurred.

(d) Subgroup 4

Performance of this 800 volts, 125^{o}C life test was successfully completed on one device and three more are in the process of being tested.

(3) Table III - Group C

(a) Subgroup 1

Additional devices will have their physical dimensions measured in July. Refer to Figure 1 in the Second Quarterly Report for the locations of the dimensions A through E.

(b) Subgroup 2

Shock and Vibration tests were performed for the first time during the MM&T Contract. Nine of the eleven devices passed. The first and third were previously degraded in a prior test and may thus have been weakened for the shock and vibration tests. The Constant Acceleration test will be scheduled in the next report period.

(c) Subgroup 3

Ten more devices were tested at reduced barometric pressure and there was no deterioration of the Final Measurement parameters from the initial values listed in Table 1a.

(d) Subgroup 4

Thermal fatigue was measured on five more of the devices. A second one degraded.

The remaining Thermal Fatigue as well as the Salt Atmosphere tests will be scheduled in the next report period.

(e) Subgroup 5

The thermal resistance of all eleven devices has been measured both before and after the frozen start tests. Ten of the eleven are satisfactory after the frozen start tests.

c. Selection of Five Samples for Delivery

Five possible groups of five samples selected from the total of eleven devices are shown in Table 2 as well as the present status of testing and the possible shipping dates indicated. Note how many tests have been completed and that most of the tests were passed. The five shippable engineering samples will be selected from one of these groups. Other samples will be retained for additional tests or analyses of failures.

Group I	All July shipments, but max. no. of remarks involved.
Group II	All July shipments, fewer remarks involved.
Group III	Partial shipments in July, balance of shipments in August.
Group IV	Partial shipments in July, balance of shipments in August and the fewest remarks involved, all parameters tested by sampling.
Group V	All July shipments but smaller samples subjected to the longtime test and the information only test will be performed on other devices (not shipped).

The latest PERT chart revision indicated a mid-July shipment of the Engineering Samples. Groups I, II or V can meet this schedule.

Table 2. Engineering Sample Shipment Schedule Alternatives

	Acceptance					Gr. A, Sub-Gr. 1-4						Gr. B, Sub-Gr. 1-4								Gr. C, Sub-Gr. 1-5								
	Vis. & Mech.	i_{FBOM}	I_H	i_{FBOM}	V_{FM}	i_{RBOM}	V_{GT}	I_{GT}	i_{RBOM}	V_{GT}	dv/dt	t_{off}	I_{FM}	V_{GT}	I_{GT}	V_{FM}	Temp. Cycle	Moist. Resis.	BL.V.L.T.	Phy. Dimen.	Shock	Vibration	Const. Accel.	Red. Bar. Press.	Salt	Therm. Fatigue	θ j-c	Possible Ship. Date	Remarks
	25 °C		125 °C			25 °C	25 °C	25 °C	125 °C	125 °C	125 °C		-25 °C		-25 °C	-25 °C													
Group I																													
N2	P	P	P	F	P	P	P	F	P	P	F	P	P$^{\Delta}$	P	P	P	P	P	IP	P	P	P		P$^{\Delta}$		P$^{\Delta}$	P	22 July	A
N3	P	P	P	F	P	P	P	F	F	P	F	P	P$^{\Delta}$	P	P	P	P$^{\Delta}$	P$^{\Delta}$	X	P	F	F		X		F	P	18 July	A,C
N4	P	P	P	P*	P	P	P	F	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	D
N5	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	B
N7	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	X	F	P	P		P$^{\Delta}$		F	P	18 July	C
Group II																													
N2	P	P	P	F	P	P	P	F	P	P	F	P	P$^{\Delta}$	P	P	P	P	P	IP	P	P	P		P$^{\Delta}$		P$^{\Delta}$	P	22 July	A
N4	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	D
N5	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	B
N6	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	P*		P	P		P		P	P	18 July	None
N7	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	X	F	P	P		P$^{\Delta}$		F	P	18 July	C
Group III																													
N4	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	D
N5	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	B
N6	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	P*		P	P		P		P	P	18 July	None
N8	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	15 Aug.	D
N11	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	15 Aug.	D
Group IV																													
N5	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	B
N6	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	P*		P	P		P		P	P	18 July	None
N8	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	15 Aug.	D
N10	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	15 Aug.	None
N11	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	15 Aug.	D
Group V																													
N4	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	D
N5	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	IP		P	P		P		P	P	18 July	B
N6	P	P	P	P	P	P	P	P	P	P	F	P	P	P	P	P	P	P	P*		P	P		P		P	P	18 July	None
N8	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	20 July	D,C
N11	P	P	P	P*	P	P	P	P	P	P	F	P	P	P	P	P	P	P			P	P		P		IP	P	20 July	D,C

*Gate Condiction B (Resistor Gate to Cathode) instead of D (open Gate).

$^{\Delta}$There was no further degradation of any parameter that may have degraded during a prior test, thus the DUT passed the subsequent test.

Key to Testing Results and Status: (Refer to Table 2)

P - Passed, including all final measurements required after the basic test.

IP - Test in pro.

F - Failed test or one of the final measurements following the basic test.

X - Cannot test for this parameter because of a prior failure.

Remarks Code: (Refer to Table 2)

A - Slightly reduced voltage was used on the 125°C Forward Blocking Current Test.

B - Verify the Salt Atmosphere results on other Engineering Samples.

C - Verify the Blocking Voltage Life Test capability from other Engineering Samples.

D - Gate Condition B, rather than D, used until an improved shorting dot pattern is utilized on future (Confirmatory) samples.

Note: It is also planned to verify the Constant Acceleration capabilities (information only test) from other engineering samples, not shipped.

The "Remarks" B and C above are consistent with the reduced test sample size of one device and 10% specified for these tests in the Confirmatory and Pilot Run phases, respectively.

d. Corrective Action

Corrective action was successful in improving the high temperature, forward blocking current and the gate current values on the later engineering sample devices. The change in passivating coating was successful in preventing voltage degradations. Additional improvements will be incorporated before the confirmatory sample phase to improve the dv/dt deficiency and to meet any other deficiencies that may become apparent during the remaining inspections. Yields will be improved prior to the pilot run.

6. Specification

The only specification change suggested is the same as in the previous report, namely, the addition of a thermal resistance test in Table II, Subgroup 1. This preliminary determination of heat-pipe efficiency could then be used to detect any internal damage, or delamination that may be caused by the frozen start (-25°C) test of Subgroup 2. This added test was performed on all of the engineering sample devices.

7. Requirement for Pilot Run

Not applicable until later in the contract.

8. Total Cost for Pilot Run

Data not available until the pilot run is completed.

9. Program Review

The PERT chart was revised and resubmitted to ECOM and MERADCOM personnel at the coordination meeting held in Lancaster in mid-May, 1977. As of 30 June 1977, the program was about three months behind schedule. The first Lancaster diffused devices were tested in the laboratory in February 1977 giving preliminary indications that the high temperature blocking voltages were not yet comparable to Somerville diffused devices. Heat-pipe and envelope sub-assembly fabrication was concluded while measures were taken to correct the wafer difficulties. Other tests and the revisions to the engineering drawings were completed. Modifications were completed on the test equipment.

Improved diffused wafers became available during the latest report period and eight additional devices were fabricated for evaluation. Shipment of the five engineering samples will thus be possible early in the next quarter of the contract.

The remaining PERT chart schedule will be reviewed to assess the impact of the delay on the subsequent Confirmatory Samples and Pilot Run phases of the contract.

CONCLUSIONS

Overall it is estimated that the engineering program was about 90% completed in the first nine months of the contract. There is concern, however, that the additional time required to achieve Lancaster-diffused wafers equivalent to Somerville's original quality may also delay the delivery schedule of the subsequent devices.

Effort expended in the third quarter was successful in correcting the wafer difficulties so that the program is nearing completion of the engineering sample phase. Early authorization of the Confirmatory Sample phase is desirable to help avoid any further delays and to possibly regain part of the lost time.

RCA is still confident of meeting the MM&TE specification requirements for the confirmatory sample and pilot run devices, because of the very favorable test results of the latest engineering sample devices.

PROGRAM FOR THE NEXT QUARTER

1. Conclude the electrical, mechanical, thermal and environmental tests on the engineering sample devices,

2. Select and deliver the five engineering sample devices following completion of all tests,

3. Issue the Test Report for the Engineering Samples,

4. Reissue the PERT chart to reflect any additional delays in the remainder of the contract, and

5. Issue the Confirmatory Sample Test Plan.

IDENTIFICATION OF PERSONNEL

The professional and skilled technical personnel who actually worked on the MM&TE project during the first three quarters have varied backgrounds, as listed in the biographical resumes included in the First and Second Quarterly Reports. No additional resumes are included in this report since the personnel assigned to the project remained unchanged in the Third Quarter.

In addition, numerous supporting personnel including managers, secretaries, purchasing agents, marketing specialists, environmental technicians, machinists, electricians, experimental tube builders, etc., have contributed to the progress made in the first nine months of the contract.

APPENDIX

Operating Procedures for the Electrical Test Equipment. Refer also to the Procedures and Block Diagrams for the Electrical Test Equipment included in the Second and First Quarterly Reports, respectively.

GATE TRIGGER VOLTAGE AND CURRENT TEST CONDITIONS

DATE: 4/28/77 RMH

REFERENCE: MIL-STD-750B, Method 4221

EQUIPMENT:

1. Hewlett-Packard 6286A Power Supply Gate Supply
2. Hewlett-Packard 6282A Power Supply Anode Supply
3. Thermometer - mercury
4. Gate Forward and Reverse Voltage and Current (GFV&GC) Test Set

PROCEDURE:

1. Set DUT into cradle inside GFV&GC cabinet for 25°C tests or into oven for 125°C Tests, observing the correct polarity. Allow time to reach temperature equilibrium in the oven.
2. Read and record the device serial no., room temperature on thermometer and oven temperature (if used).
3. Ground the negative posts of both power supplies.
4. Connect the respective power supplies with the correct polarity to the anode and gate jacks on test circuit.
5. Set the mode switch to "Forward" and turn on the two power supplies.
6. Set the anode voltage to 6 volts on the circuit panel meter.
7. Advance the gate voltage to the point where the anode voltage suddenly drops to a low value. Repeat this a few times (after depressing the reset button) to be sure of the reading just prior to the drop in voltage.
8. Record both the gate voltage and current observed in step #7 just prior to conduction. Adjust the meter range switches as required for accurate readings.

GATE TRIGGER VOLTAGE AND CURRENT TEST CONDITIONS (Cont.)

PROCEDURE: (Cont.)

9. Turn-off power supplies and remove the DUT from the test set or oven (using thermal insulating gloves).

CALIBRATION DATES:

Equipment	Date
Gate Voltmeter	Prior to installation in December 1976
Gate Ammeter	Prior to installation in December 1976

GATE TRIGGER VOLTAGE AND CURRENT AT -25°C AND ON-STATE VOLTAGE AT -25°C TEST PROCEDURE

DATE: 5/6/77 RMH/RER

REFERENCE: MIL-STD-750B, Method 4221 and 4226,

EQUIPMENT:

1. Environmental Chamber, American Research Model 50H36-100300 or equivalent.
2. Hewlett-Packard 6286A Power Supply Gate Supply
3. Hewlett-Packard 6282A Power Supply Anode Supply
4. Simpson Therm-O-Meter Model 388 and Plug-in Thermocouple
5. Gate Characteristics Test Set
6. Minimite to read millivolts and heat-pipe temperatures.
7. For On-State equipment - See On-State Voltage Test and omit thermometer and pitot tube.*

PROCEDURE:

1. Attach DUTs in parallel to copper bus bars of test fixture (insulated) to support the DUTs and to supply the On-State current from outside the environmental chamber.
2. Connect all DUT cathode leads (red) together to a common wire.
3. Connect a separate gate lead, a separate anode lead, and a separate thermocouple to each DUT.
4. Tag these leads and thermocouple leads for each DUT to provide identification outside of the chamber of the serial number and terminal to which each is connected.
5. Put the wires and the copper bus bars through the hole from the inside out and push the foam insulation and its supporting discs into the hole. This should be tight enough to hold the DUTs in position away from the chamber interior walls.

GATE TRIGGER VOLTAGE AND CURRENT AT -25°C AND ON-STATE VOLTAGE AT - 25°C TEST PROCEDURE (Cont.)

PROCEDURE: (Cont.)

6. Before closing the chamber, run the gate tests at room temperature to check all of the connections.

7. Make sure the thermocouples are securely against the heat-pipes of their respective DUTs.

8. Run the On-State Voltage Test at reduced current on each DUT briefly to see that each is hooked up properly. Caution: Do not overheat the DUTs since no cooling air is provided for this test.

9. Close chamber door and cool to -25°C (-13°F). Allow adequate time for the DUTs to achieve temperature equilibrium at -25°C.

10. When the specified temperature is reached, run the gate characteristics test on all of the DUTs first. Record all necessary V_{GT} and I_{GT} values. Then run the On-State voltage test and read and record the peak voltage on the oscilloscope when the temperature is between 25°C and 100°C. Be sure to wait for each DUT (to be tested for On-State voltage) to return to -25°C before applying the voltage. Also, replace the one-half-ohm resistor between the gate and anode with a short circuit to enable the DUT to conduct during the On-State test. Caution: Do not exceed 100°C on the heat-pipes.

11. Turn off equipment and remove DUTs from chamber only after the chamber has returned to room temperature. This will avoid excessive condensation.

CALIBRATION DATES:

Equipment	Date
(Refer to "On-State Forward Voltage Test"* and "Gate Trigger Voltage and Current Test" procedures.)	

*Included in Appendix C of the Second Quarterly Report, page C8.

REVERSE GATE CURRENT TEST PROCEDURE

DATE: 5/8/77 RMH

REFERENCE: MIL-STD-750B, Method 4219

EQUIPMENT:

1. Hewlett-Packard Type 6286A Power Supply
2. Thermometer, mercury
3. Gate Forward and Reverse Voltage and Current (G.F.R.V.C.) Test Set

PROCEDURE:

1. Set DUT in cradle inside G.F.R.V.C Test Set Cabinet, observing the correct polarity.
2. Read and record room temperature on the thermometer and record the serial number of the device under test (DUT).
3. Ground the negative post of the power supply and plug the power supply into the Gate Terminals on the test set. The anode supply is not used for this test.
4. Turn Mode Switch to "Reverse" position and turn on the power supply.
5. Set gate voltage to 5 volts and read and record the reverse gate current. Readjust meter range switch, if necessary.
6. Turn-off power supply and remove the DUT from the test set.

CALIBRATION DATES:

Equipment	Date
Gate Voltmeter	Prior to installation in December 1976
Gate Ammeter	Priot to installation in December 1976

BLOCKING VOLTAGE LIFE TEST PROCEDURE

DATE: June 23, 1977

REFERENCE: SCS-477, para. 4.6.1

EQUIPMENT:

1. Blocking Voltage Life Test Set, 60 Hz, 800 volts (BVLT)
2. Minimite Thermocouple Meter
3. Temperature Controlled Oven
4. Oscilloscope Type 536 Tektronix or equiv.
5. Mercury Thermometer

PROCEDURE:

1. Fasten the thermocouples for the Minimite and the temperature meter onto the DUT heat-pipe which will be at ground potential in the oven.
2. Put the DUT into the electrical terminal clips of the mounting rack in the oven. Connect the ground and high voltage leads to the appropriate terminals on the rack.
3. Set the correct gate condition and apply the 800 V peak voltage to the device. Note the oven door must be closed to activate the interlock.
4. With the DUT in the oven and the 800 V applied by the BVLT Test Set, bring the oven temperature up to about 115°C, as read on the thermometer. The DUT leakage current losses will probably increase the DUT case temperature to 122-125°C. If not, readjust the oven temperature so that the DUT will be at 122-125°C.
5. Read and record the hour meter, temperatures and voltage. Monitor the test periodically during the 500 hours testing interval and readjust operating conditions, as required.
6. At the end of the test interval, cool oven, carefully remove the DUT and perform the specified Final Measurements.

CALIBRATION DATES:

Equipment	Date
Tek 536 Test Set Meters	19 May 1977 Calibrated prior to installation

TURN-OFF TIME TEST PROCEDURE

DATE: June 28, 1977

REFERENCE: MIL-STD-750B, Method No. 4224

EQUIPMENT:

1. On-State Current Pulse Power Supply (OCPS)
2. Reverse Current Pulse Power Supply (RCPS)
3. Fast Rise Forward Voltage Power Supply (FVPS)
4. Tektronix Type 564B Oscilloscope, or equivalent.
5. 100:1 Voltage Divider, Tektronix Type P6007
6. Current Transformer 0.5 V/1 Amp, Pearson Model 150
7. (2) H.P. 214A Power Pulser Generators
8. H.P. 8015A Dual Output Pulse Generator
9. Tektronix Type 3A6 & 3B3 Plug-In Units, or equivalent

PROCEDURE:

1. Install the DUT in the socket of the interlocked high voltage enclosure and connect the gate lead.
2. Apply approximately 100 Amperes of peak forward current from the OSCPS.
3. Apply sufficient reverse current from the RCPS to commutate the DUT off. Adjust the pulse phasing to secure at least 100 µs duration of the 100 amperes of forward current before turn-off. Readjust values as required.
4. Apply the 800 volts of peak forward voltage from the FVPS at least 150 µsec after the commutation. Vary this interval (reduce 150 µs) until the DUT no longer remains off, as indicated by a severe loading of the 800 volts.
5. Read and record the time interval just prior to the severe loading. This is the turn-off time.

6. Turn-off all supplies and carefully remove the DUT from the socket.

CALIBRATION DATES:

Equipment	Date
Tek 564B, 3A6 & 3B3	13 July 77

REPETITIVE SURGE CURRENT TEST PROCEDURE

DATE: June 30, 1977

REFERENCE: MIL-STD-750B, Method No. 4066

EQUIPMENT:

1. Tektronix Type 564 B Storage Oscilloscope or equivalent

   Set-Up: Allow 20 minutes warm-up time with plug-ins inserted. Storage function is turned off until just prior to measurements.

2. Tektronix Type 3B3 Time Base Plug-In Unit or equivalent

   Set-Up: Sweep - 5 msec/div.
   Trigger - Normal, +, AC, Int.
   Trigger Level - Slightly positive

3. Tektronix Type 3A6 Preamp Unit or equivalent

   Set-Up: Chop mode
   Trigger - Channel 1 only
   Channel 1 - (Cable from current shunt resistor)
   - Vertical sensitivity - 0.5 V/div.
   - D.C. input
   - Inverted display
   - Trace centered vertically

   Channel 2 - (Cable from voltage divider)
   - Vertical sensitivity - 2.0 V/div.
   - D.C. input
   - Trace centered vertically

4. 12 V, 4000 A Surge Current Power Source

   -DUT Test Socket with forced air cooling
   -100:1 voltage divider
   -4000 A/V current shunt resistor

5. 4 V, 250 A Average A.C. Heating Current Power Source

6. Surge Current Control Cabinet with Integral 0 to 800 V Peak Applied Reverse Voltage

7. Integral Connecting Cables and Control Wires

8. Mechanical 2 Hour Timer

PROCEDURE:

1. Mount DUT in the test socket with anode to ground terminal - connect cathode cable, voltage divider and gate lead.

2. Close interlocked cabinet door.

3. Turn on heating current supply and raise current to 250 amperes average.

4. Allow five minutes for thermal stabilization.

5. Record ambient temperature on data sheet.

6. Turn on surge current supply and advance the primary voltage to 330 volts as read on the panel meter.

7. On the control cabinet, turn on the reverse voltage and advance the variac control to 590 volts on the A.C. panel voltmeter.

8. Check 'scope trace centering (by switching momentarily to auto trigger). Then turn on storage function.

9. Note timer reading and press "start surge" switch. There will be about a four second delay before the surge occurs.

10. Observe waveform on the 'scope.

11. The current waveshape (1st downward moving 60 Hz half cycle) should be at least two divisions or 4000 amperes peak. Verify a minimum duration of 7 ms at the base of the sinewave.

    The upward moving 2nd half cycle should be at least four divisions or 800 volts reapplied reverse voltage. Record the actual values of both the peak current and peak voltage.

12. If both waveforms show no discontinuities, record as a successful surge.

13. Repeat this surge sequence at one minute intervals for ten total surges. This completes the required test.

14. In the event the fail indicator lamp comes on and/or the reverse voltage shows a breakdown on the 'scope, reduce the reverse voltage by 100 volt intervals until a successful surge is completed. Record this voltage and complete data at this level.

15. Turn off all voltage supplies and discharge the high voltage terminals with a grounding wand.

16. Carefully remove the DUT from the test socket and perform the specified "Final Measurements."

CALIBRATION DATES:

Equipment	Date
1. Tektronic 564B main frame, storage oscilloscope	7/13/77
2. Tektronic Type 3B3 time base, plug-in unit	7/13/77
3. Tektronix Type 3A6 Preamp Plug-In Unit	7/13/77
4. Westinghouse style 703932 200 A, 50 mv current shunt	8/9/77
5. Resistive voltage divide composed of a 51K, 5% 2 watt carbon resistor and a 510 ohm, 5% 2 watt carbon resistor filed and sealed to produce 100:1 ±1% ratio	8/8/77
6. 0 to 500 A.D.C. current meter, 0 to 50 mv movement, Westinghouse type FX382 TBS S/N L8327 with 50 mv, 500 A current shunt style 282640E	8/8/77

HOLDING CURRENT TEST PROCEDURE

DATE: May 12, 1977

REFERENCE: MIL-STD-750B, Method 4201

EQUIPMENT:

1. Holding Current Test Set (HCTS)
2. Hewlett Packard 6282A Power Supply
3. Hewlett Packard 6286A Power Supply

PROCEDURE:

1. Place DUT in socket of the HCTS and connect the gate lead.
2. Connect the 6282A as the anode supply (for one ampere). Connect it to the left pair of terminals.
3. Use the 6286A as the gate power supply for five volts.
4. Turn the range switch to 1000 mA and the anode supply to the voltage as needed for 1.0 ampere.
5. Set the gate supply to 5 volts and press the gate trigger button for two seconds to turn on the DUT.
6. The anode resistance knob is then advanced immediately to reduce the current to 500 mA and then slowly clockwise until the DUT turns off. A lower range of current reading may be necessary.
7. The anode voltage and other test conditions may have to be reset after the range is changed to maintain a large enough anode variable resistance to turn off the DUT before the resistor is rotated to the end of its travel.
8. Read and record the anode current just prior to the DUT stopping conduction. This is the holding current value.
9. Carefully remove the DUT from the HCTS.

CALIBRATION DATES:

Equipment	Date
Power Supply Meters	Calibrated when received from vendor in early 1977,
Holding Current Ammeter	Calibrated prior to installation

THERMAL FATIGUE TEST PROCEDURE

DATE: 5/13/77 RMH

REFERENCE: SCS-477, Method para. 4.6.2

EQUIPMENT:

1. Tektronix Type 536 or equivalent oscilloscope
2. Thermometer - mercury
3. NWL Power Supply; 3000 Amps AC, 10 V AC; PP #096893 (Main P.S.)
4. Two Rustrak Recorders, Model 2155A and two Iron Constantan TC's
5. Two 500 Amp shunts with meter to read DC Amps for each
6. Thermal Fatigue Test Control (CLT) Cabinet with Timers and Counters
7. Duotrol Cycle Timer
8. Dwyer Pitot Tube - level before using.

PROCEDURE:

1. Read and Record Ambient Temperature on Thermometer.
2. Attach the iron-constantan thermocouple to the hottest heat-pipe on each of the DUTs and on one attach the protection thermocouple next to the iron-constantan thermocouple. Note: The thermocouple wires should be on the same side of the heat-pipe as the gate and emitter leads (i.e., out of cooling air flow).
3. Attach one DUT (or two DUTs in inverse parallel) on the copper plate with the gate and auxiliary emitter wires oriented away from the cooling blower duct.
4. Attach the heavy copper cables to the DUTs. The adjustable, high current resistor should be in series with the DUT having the lowest on-state voltage.

5. Insert the DUTs into the end of the air cooling duct and attach the copper plate to the bakelite with 1/4-20 machine screws.

6. Attach the front DUT emitter (red) and gate (white) leads to the top Vectrol terminals on the terminal strip provided on the air duct and the back DUT leads to the bottom terminals.

7. Plug the over-temperature protecting thermocouple into the plug (female) of the main power supply. Check the red needle setting on the dial on the front of the main P.S. to see that it is 80^{o}C above the black needle. Reset, if necessary.

8. Attach the double heavy cables to the copper plate common to both DUTs.

9. Plug the Duotrol Cycle Timer into the CLT cabinet and the Vectrol Gate Supply as well as the two Rustrak recorders into the proper outlets on the back of the CLT cabinet. Plug the CLT cabinet power cord into a 127 VAC outlet.

10. Plug the Jones interlock plug from the CLT cabinet into the plug (female) between the secondary leads of the main P.S.

11. Connect the air flow interlock and then plug the main P.S. into 440 VAC, 3 phase and turn it on.

12. Set the CLT cabinet to "Continuous mode" and turn the blower on at maximum cooling flow (blast gate open).

13. Advance the voltage of the main P.S. to where the pilot light on the Duotrol, the Continuous Run, the Trigger "off" (or "on") and the Heating Supply "On" pilot lights turn on. Turn the Recorders on (switch on back of case) and the Vectrol mounted on the side of main P.S.

14. Push the reset (red) button on the C.L.T cabinet if the Duotrol is in the "off" cycle and advance the current on the shunt ammeters to 100 Amps. Time the "on" and "off" intervals of the Duotrol and reset, if necessary, for two minutes each.

15. With the oscilloscope across one of the DUTs, adjust the knob on the Vectrol to get the maximum conduction angle wave shape. Alternatively, a true RMS meter reading can be maximized as the indication of maximum conduction angle.

16. Advance the current to 250 Amps and if there is a difference between the two meters, change the length of the high current resistor in series with the one DUT. Adjust total current series resistor to achieve the six volts minimum a.c. voltage specified. Be sure to make the adjustment only during the "off" cycle.

17. Readjust the current to 250 amps at the end of the 2 min "on" cycle. This must be checked from time to time to correct for thermal effects until there is no change from cycle to cycle.

18. Check the peak temperature on the Rustrak recorders and adjust the blower blast gate opening to bring the heat-pipe temperatures to within the specified maximum limits. Be sure to maintain at least 100 cfm of cooling air.

19. Set the Interval Timer on the CLT cabinet to 14.2 hours and switch to the "Interval mode." Press the red button on the Interval Timer to start the 200 + cycles sequence. Be sure the minimum temperature is within the specified tolerance.

20. After test is completed, turn main P.S. variac (black wheel) back to zero and push the off button; then turn off the recorders, Vectrol and CLT cabinet power switch. Lastly turn off the blower.

21. Remove the portion of the recorder tapes containing the temperature cycles, verify that the maximum and minimum temperatures were achieved on at least 20 cycles; if so, label and file the charts by device serial number.

22. Proceed with the required Final Measurements.

CALIBRATION DATES:

Equipment	Date
Tek. 536	11/9/76
Rustrak 2155A & Thermometer	(Calibrated periodically at 100°C in boiling water)
Shunts and meters	(Calibrated prior to construction of test equipment)
Timer	(Calibrated in Testing Procedure, above)

REDUCED BAROMETRIC PRESSURE (CORONA) TEST PROCEDURE

DATE: May 23, 1977

REFERENCE: MIL-STD-750B, Method No. 1001

EQUIPMENT:

1. Reduced Barometric Pressure Power Supply and Vacuum System
2. Tektronix Type 536 Oscilloscope or equiv.
3. Tektronix Type 600 High Voltage Probe 100:1
4. Pressure Gauge - Wallace Tiernon Mod. #FA160
5. Pressure (Vacuum) System PP #97279
6. GE Timer

PROCEDURE:

1. Insert DUT in chamber between two connectors, one of which holds off 1000 VAC at the reduced pressure to be used. The second connector is grounded.
2. Connect the power supply and oscilloscope leads to the two connectors with the high voltage probe on the high voltage connector. Close the vacuum bell.
3. With the Foreline and Roughing valves closed, and, with the vacuum bell at room temp. and pressure, advance the applied voltage to 800 VAC peak forward and reverse.
4. Close the air inlet and switch the roughing valve to "open" and allow pressure to pump down to 15 mm of Hg. Hold this pressure for one minute by switching the roughing valve to "close." Use the timer for the one minute interval.
5. After one minute, open air bleeder valve between the gauge and the system air inlet. Allow the DUT to return to atmospheric pressure. Record any arcovers or excessive corona that occurred during the testing sequence.

6. Turn off the 800 VAC supply and carefully remove the DUT from the system. If corona was observed, inspect the device under test for any physical damage that may have occurred. Perform the specified "Final Measurements."

CALIBRATION DATES:

Equipment	Date
Tek. 536	19 May 1977

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